

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE PATENT APPLICATION

Applicant:

Bernstein et al.

Serial No.: 10/710641

Filed:

07/27/2004

Atty. Docket: BUR920020035US1

Title:

ERROR CORRECTING LOGIC SYSTEM.

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.56, 1.97, 1.98

Honorable Commissioner of Patents and Trademarks Washington, D. C. 20231

Sir:

Applicants submit herewith form PTO-1449, listing patents, publications, or other information of which they are aware which they believe may be material to patentability pursuant to 37 CFR 1.56(b), and in respect of which there may be a duty to disclose under 37 CFR 1.56(a), together with legible copies of the patents, publications, or other information listed.

While the items submitted with this Information Disclosure Statement may be material to patentability pursuant to 37 CFR 1.56, in accordance with 37 CFR 1.97(h) it shall not be construed to be an admission that any patent, publication, or other information cited is "prior art" or is material to patentability for this invention unless specifically designated as such. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other information material to patentability, as defined in 37 CFR 1.56(b), exists.

Respectfully submitted,

Date: 7-30-04

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	REF	DOCUMENT NUMBER	DATE	COUNTRY		CLASS	SUBCLASS	Translation YES NO	
		JP6216756	08/1994	Japan					
		EP0147598A1	07/1985	ЕРО					
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